

REMARKS

This application has been reviewed in light of the Office Action dated May 13, 2009. Claims 1–4, 6–8, and 10–24 are pending in the application. Claims 2–4, 7–8, and 11–24 have been withdrawn pursuant to a restriction requirement. Claims 1, 6, and 10 have been amended, with the amendments to claims 6 and 10 merely correcting the claim dependencies. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

Claims 1, 6, and 10 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

The Examiner objected to the “noise blocking resistor” language of the claim, which has been removed without prejudice in the present amendment. It is therefore respectfully asserted that the section 112 rejection is moot. It is therefore believed that claims 1, 6, and 10 are in condition for allowance.

Additionally, claim 1 has been amended to make reference to bypass capacitors and a decoupling resistor. These amendments are well supported by the specification. *See, e.g.*, p. 8, lns 21–25. Claim 1 as amended recites, *inter alia*, “a first bypass capacitor connected in parallel between an output port of the amplification means and ground port to function as a filter; a second bypass capacitor connected parallel to the first bypass capacitor to perform an EM-noise-filtering and ESD-blocking function; and a first decoupling resistor connected serially between an output port of the first bypass capacitor and an output port of the second bypass capacitor to perform a decoupling function, so that the EM-noise-filtering/ESD-blocking section has a shape of a character ‘Π’.”

U.S. Patent No. 6,978,029 to Ikeda (hereinafter “Ikeda”), the art previously cited by the

Examiner, does not show these features. The Examiner cited FIG. 3 of Ikeda as disclosing the elements of claim 1, but it is clear that, while claim 1 recites two *bypass* capacitors, Ikeda shows only one. Ikeda furthermore fails entirely to show a *decoupling* resistor, or that such a decoupling resistor might be connected serially between the respective output ports of two bypass capacitors.

Furthermore, and contrary to the Examiner's earlier assertions, *none* of the figures in Ikeda shows a 'II' configuration. FIG. 4, which the Examiner cites, does not show a resistor being arranged serially between the output ports of the capacitors, but instead shows a resistor being serially coupled to only one capacitor, making it parallel to the second capacitor. As those skilled in the art are well aware, the difference between a parallel arrangement and a series arrangement in a circuit leads to substantial differences in the behavior of the circuit, so the Examiner's assertion that "it is a matter of design choice how this section is shaped" (Office Action of 10/28/2008, p. 5) is clearly inaccurate.

Indeed, the portion of Ikeda which the Examiner has focused on in an attempt to show a 'II' configuration, i.e., the resonance circuit shown in FIG. 4, is designed to cut off a direct current and a parallel resonance. *See* Ikeda, col. 6, lns 53–62. Thus the structure of Ikeda's FIG. 4 would be wholly inappropriate for blocking noise. It is therefore clear that the 'II' structure recited in the present claims is not merely a matter of "design choice," but instead is a legitimate structural element which must be accounted for.

For at least the above reasons, it is respectfully asserted that Ikeda neither discloses nor suggests all of the elements of claim 1. It is therefore believed that claim 1 is patentable over Ikeda. Because claims 6 and 10 depend from claim 1 and include all of its elements, it is believed that claims 6 and 10 are also patentable over Ikeda.

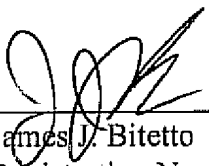
In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

The Office is authorized to charge a three-month extension fee of \$555 to the applicant's representatives' Deposit Account No. 50-1433. It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives' Deposit Account No. 50-1433.

Respectfully submitted,

Date: 11/13/69

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